

IN THE TITLE:

Please change the title to --DUAL ASSOCIATIVE-CACHE DIRECTORIES ALLOWING SIMULTANEOUS READ OPERATION USING TWO BUSES WITH MULTIPLEXORS, ADDRESS TAGS, MEMORY BLOCK CONTROL SIGNALS, SINGLE CLOCK CYCLE OPERATION AND ERROR CORRECTION--.

IN THE CLAIMS:

Please delete Claims 2, 5 and 11-13. Please amend the remaining claims as follows (all pending claims are presented whether or not amended):

1 -- 1. (amended) A method of accessing values stored in a cache used by  
2 a processor of a computer system, comprising the steps of:

3 loading a plurality of memory blocks from a memory device connected  
4 to the processor via a system bus into respective cache lines of the cache;

5 writing address tags associated with the memory blocks into first and  
6 second cache directories of the cache, wherein the first and second cache  
7 directories are redundant, and said writing step writes a given one of the  
8 address tags to a specific line of the first directory and to a specific line of the  
9 second directory that corresponds to the specific line of the first directory; and

10 reading a first memory block from the cache using the first cache  
11 directory, while reading a second memory block from the cache using the  
12 second cache directory, wherein the first and second memory blocks are read  
13 in a single clock cycle of the processor.

1 2. (deleted)

1 3. (unchanged) The method of Claim 1 wherein the cache has a single  
2 cache entry array, and said step of reading the first memory block while reading  
3 the second memory block includes the steps of:

4 constructing a first control signal for the first memory block based on a  
5 first location

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